Senior Firmware Engineer

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Company: Advanced Micro Devices, Inc

Location: Vancouver

Category: computer-and-mathematical

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Knowledge of SystemC, Verilog and Python. VCS simulation and debug experience. Strong understanding of memory controllers, PHYs, and dram protocols. Applied knowledge of JEDEC standards in relationship to firmware development and debug. Laboratory experience, including the use of equipment: oscilloscopes, logic analyzers, etc. to debug and triage firmware and lab bring up issues. EDUCATION: Bachelor's degree in Electrical or Computer Engineering and relevant experience, or Master's or PhD degree in Electrical or Computer Engineering with relevant experience. LOCATION: Vancouver, BC Canada #LI-RD1 #LI-HYBRID Benefits offered are described: AMD benefits at a glance. AMD does not accept unsolicited resumes from headhunters, recruitment agencies, or fee-based recruitment services. AMD and its subsidiaries are equal opportunity, inclusive employers and will consider all applicants without regard to age, ancestry, color, marital status, medical condition, mental or physical disability, national origin, race, religion, political and/or third-party affiliation, sex, pregnancy, sexual orientation, gender identity, military or veteran status, or any other characteristic protected by law. We encourage applications from all qualified candidates and will accommodate applicants' needs under the respective laws throughout all stages of the recruitment and selection process.FIRMWARE ENGINEER The Person: You have interested in architecture model development, testing as well as firmware coding. You are a team player who has excellent communication skills, strong analytical and problem-solving skills and willing to learn and ready to take on problems. A global mindset and ability to work in multi-site environment are keys to being successful in this role. The Role: As a member of the Memory PHY architecture modeling team, you will help build the next memory PHY model used for firmware development and boot loader verification. The architecture model is a reusable IP and its variances are used in many AMD products including graphic, client, and servers. It is a challenging position that involves working at a fast pace of innovation on the cutting edge of technology. REQUIRED SKILLS: Excellent knowledge of C, C++, and any scripting language Ability to adapt learn new toolsets and framework. Pre-silicon and post-silicon experience developing and debugging firmware, both on simulation/emulation/FPGA platforms and real hardware. Experience with DDR/JEDEC standard IP, DDR PHY, or Memory Controller firmware development. Strong understanding of computer organization/architecture. PREFERRED EXPERIENCE DESIRED: Knowledge of SystemC, Verilog and Python. VCS simulation and debug experience. Strong understanding of memory controllers, PHYs, and dram protocols. Applied knowledge of JEDEC standards in relationship to firmware development and debug. Laboratory experience, including the use of

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